

ABSTRACT OF THE DISCLOSURE

A partial circuit of an encoding circuit for realizing a first error correction encoding algorithm and a partial circuit of an encoding circuit for realizing a second error correction encoding algorithm are shared to realize these two algorithms by one error correction encoding circuit. A partial circuit of a decoding circuit for realizing a first error correction decoding algorithm and a partial circuit of a decoding circuit for realizing a second error correction decoding algorithm are shared to realize these two algorithms by one error correction decoding circuit. A plurality of error correction encoding^{& decoding} algorithms can therefore be realized by a simple and inexpensive circuit. [A plurality of error correction decoding algorithms can therefore be realized by a simple and inexpensive circuit.]

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